Equivalent Model for Calculating Fault Current from Inverter-Interfaced Renewable Energy Generators

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ABSTRACT. With decarburization of the electrical grid, the penetration of renewable energy generators (REGs) is increasing. Consequently, the operating environment of the electrical grid is greatly altered and the existing protection system for the electrical grid cannot adapt to the new environment. In order to solve the existing protection problems, the equivalent model for calculating short-circuit current of the REGs should be built. The calculation model depends on the fault current characteristics of REGs that are different from the conventional generators (synchronous generators). The short-circuit current characteristics of REGs are related with the corresponding inverter control strategies. However, the strategies are diverse from manufacturer to manufacturer and are unknown to the public. As a result, it becomes difficult to reveal the fault current characteristics and realize fault current calculation without knowing the control strategies. In this paper, the focus is on the fault current characteristics and their calculation models of inverter-interfaced REGs (IIREGs). To reveal the relationship between the inverter's control strategies and the IIREG's short-circuit current characteristics, a coordinated control strategy for gird-tie inverter and DC-link chopper is proposed. The main factors affecting the transient and steady-state short-circuit currents are analyzed and revealed for IIREGs. Further, the calculation model of the steady-state short-circuit current from IIREGs is established, which is independent of the specific inverter's control strategies. Finally, based on the experimental test bench, both the fault ride through (FRT) capability and short-circuit current model of IIREG are verified. The results can be used for assessing and improving the relay protection strategies of the electrical grid with lots of IIREGs.

Keywords: Asymmetrical fault-ride-through control, fault current characteristics, inverter-interfaced renewable energy generators, solar power, wind power

1. Introduction

In order to effectively mitigate global energy-related CO_2 emissions, renewable-energy penetration in electrical grids is expected to spectacularly grow (Dong et al., 2012; Tan et al., 2013; Zheng et al., 2014; Dong et al., 2016; Clack et al., 2017). The integration topology and generation principle of renewable energy generators are different from the ones of traditional synchronous generators (Yaramasu et al., 2015). It brings challenges to the existing protection system of electrical grids (He et al., 2012; Jia et al., 2017). To safely clear short circuit faults from the electric power system, the existing protection relays are usually designed based upon the fault characteristics of fundamental frequency currents. However, with high penetration of the renewable energy generators (REGs), the fundamental fault current characteristics are altered greatly (Muljadi

et al., 2013; Kong et al., 2014). It leads to the protection relay's incorrect operation (He et al., 2012), such as disconnecting the non-fault sections, remaining the fault for a relative long time. Consequently, the electrical grid with a lot REGs becomes unstable and unsafe.

To address the existing protection issues of the electrical grid with high penetrations of REGs, two major researches must be done. The first one is how to understand and derive the fault current characteristics and their calculation models of the REGs. On the other hand, it is also important how to assess and improve the existing protection principles. The fault current characteristics and their calculation models are the basis for developing the protection principles. This paper mainly studies on the fault current characteristics and their calculation model of the inverter-interfaced REGs (IIREGs). The IIREGs have been widely applied in the actual wind farms, photovoltaic power stations, fuel cell, and micro-turbine and so on because of the fast and flexible control provided by their power-electronic devices.

For IIREGs, the generation units are connected into the electrical grid only through the inverters. Hence, the IIREGs' fault current depends mainly on the inverter's dynamic be-

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haviors. The behaviors are determined by the response of the inverter's controller to a sudden fault (Darwish et al., 2013). The control schemes used in practice are diverse and unknown to the public. As a result, it becomes a puzzling problem to reveal fault current characteristic and derive the current expression without knowing the control strategies.

In the REGs' development early years, Baran et al. (2005) and Nimpitiwan et al. (2007) studied on the fault current contribution from IIREGs taken into account the normal grid-connected control strategies of the inverter. At that time, the fault ride through (FRT) requirement for REGs was not still issued. Thus, the research results are inadequate with the FRT requirement (The Standardization Administration of the People's Republic of China, 2011; E.ON Netz GmbH, 2006). Furthermore, Plet et al. (2010) and Muljadi et al. (2010) revealed the fault current characteristics of IIREGs by considering the inverter's FRT control strategy. The aforementioned studies depend entirely on the designated control strategy, so the fault current characteristics show diversity. In addition, the research works adopt the simulation analysis or physical experimentation method. Consequently, the obtained results are not sufficient and are unable to analytically calculate the short-circuit current.

To study the fault current calculation of IIREGs, Fischer et al. (2011) and Hooshyar et al. (2013) proposed the fault current expression of IIREGs system by treating the generators as a controlled current source. The current source model is established under assumption of constant output power before and after a grid fault, and it does not allow for the dynamic reactive power regulation of IIDGs. In fact, the regulation is important for IIREGs to ride through different types of grid faults. Hence, Wang et al. (2015) established the controlled current source model that provides reactive power support for the IIREGs. However, these studies mentioned above cannot provide theoretical explanation for representing the IIREGs as the controlled current sources. Jia et al. (2017) derived the formula for positive- and negative-sequence currents from the IIREGs during the steady-state period of a fault in consideration of the grid-tied inverters control (Rodriguez et al., 2007; Castilla et al., 2010; Miret et al., 2012). However, the grid-tied inverters' capacity constraint was not considered. The practical inverters' maximum allowable capacity is limited (Mortazavian et al., 2016). The capacity constraint affects the current contribution from the IIREGs under the different faults. Furthermore, the IIREGs' short-circuit current was not theoretically analyzed for the transient period of a fault in the existing literatures.

Therefore, the objective of this study is to analyze theoretically the fault current characteristics of the IIREGs and fur-
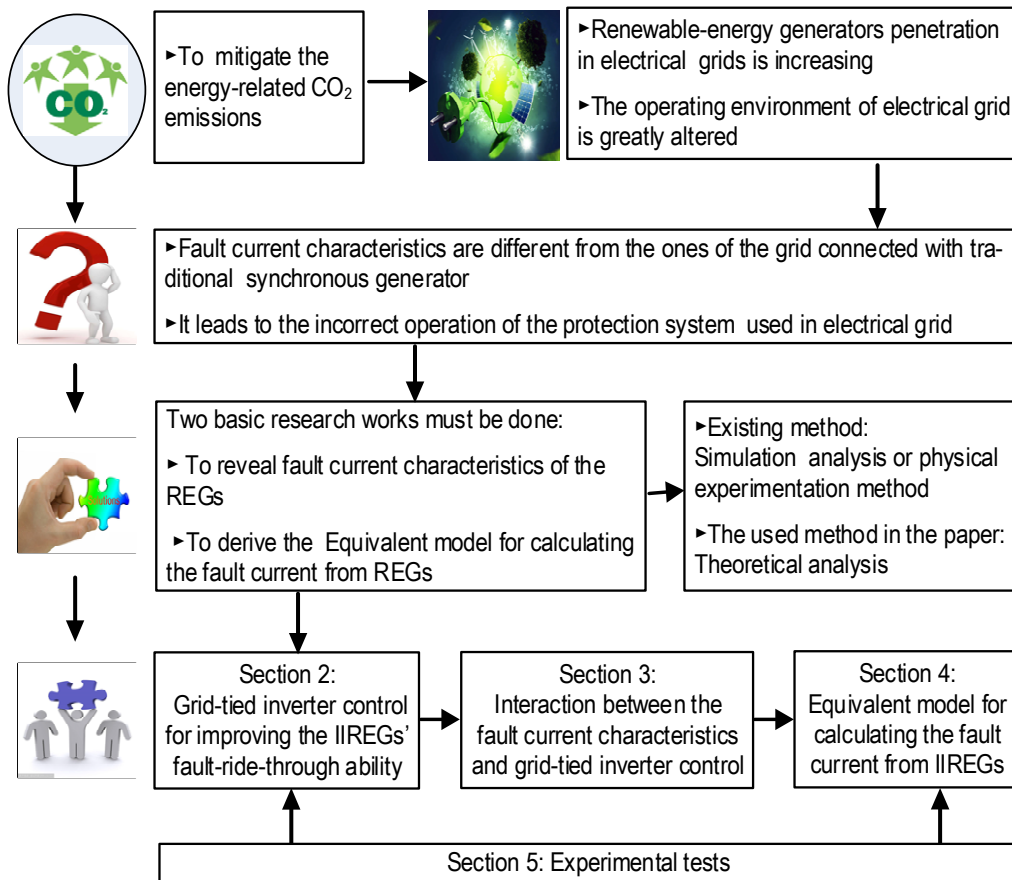

Figure 1. The paper's main contribution and logical structure.

ther derive a unified expression of the fault current. Because of the interaction between the fault current characteristics and the inverter control strategy, the inverter control strategy is developed to ensure the IIREGs ride through different faults. Figure 1 shows the contributions of this study, the methods and the structure of the paper.

The remaining paper is organized as follows. Section 2 discusses the improved FRT control strategy for the grid-tied inverter. In Section 3, the relationship between the inverter's control strategy and the IIREGs' fault current characteristics are theoretically revealed during the faults. In Section 4, the mathematical expression of steady-state fault current is derived in consideration of the reactive power support and inverter capacity constraint of IIREGs during FRT. In Section 5, both the FRT control strategy and fault current expression of IIREG are verified based on the experimental test bench. Conclusions are drawn in Section 6.

2. Advanced FRT Control Strategy of IIREGs

In order to reveal the IIREGs' fault current characteristics, the control strategy for grid-tied inverter is here developed under the faults. Although the vector-oriented current feedback control strategies have been widely used for solving the FRT problem (Hansen et al., 2009), they are suitable only for the symmetrical fault conditions and cannot improve the FRT ability under the asymmetrical faults. Some FRT control strategies especially for asymmetrical grid faults, such as the vector current control with feed forward negative-sequence grid-side voltage (Rioual et al., 1996), dual vector current control (DVC-C) in a positive and negative synchronously rotating frame (Chong et al., 2008), and proportional-resonant control in a two-phase stationary frame (Hu et al., 2008), are designed to adjust the IIREG operating features. However, the strategies do not consider the inverter over-current and DC-link over-voltage problems. Consequently, the strategies cannot achieve FRT requirements under severe asymmetrical faults. In the section, the advanced FRT control strategy is studied to provide a solution to the inverter over-current and DC-link over-voltage.

2.1. Influence of Severe Asymmetrical Fault on IIREG

The integration topology of an IIREG is shown in Figure 2. The generation unit is connected into the electrical grid only through a grid-tied inverter.
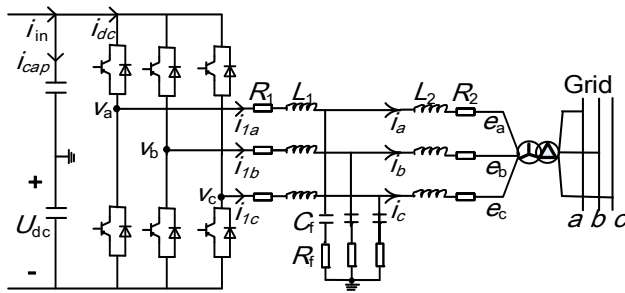

Figure 2. Main topology of a grid-connected IIREG.

Under the asymmetrical faults, the instantaneous active and reactive power outputs provided by the IIREG can be expressed as:

$$\begin{cases} P_{out} = 1.5(P_{out}^o + P_{out}^c \cos 2\omega t + P_{out}^s \sin 2\omega t) \\ Q_{out} = 1.5(Q_{out}^o + Q_{out}^c \cos 2\omega t + Q_{out}^s \sin 2\omega t) \end{cases} \quad (1\text{-}1)$$

where $P_{out}^o(Q_{out}^o)$, $P_{out}^c(Q_{out}^c)$, $P_{out}^s(Q_{out}^s)$ represent the average dc component, sinusoidal component, cosine component of instantaneous active power (or instantaneous reactive power). ω is the grid frequency. These components can be represented with the grid-side voltage and output current in synchronously rotating dq reference frame as follows (Yongsug et al., 2006)

$$\begin{cases} P_{out}^o = e_d^p i_d^p + e_q^p i_q^p + e_d^n i_d^n + e_q^n i_q^n \\ Q_{out}^o = e_q^p i_d^p - e_d^p i_q^p - e_q^n i_d^n + e_q^n i_d^n \\ P_{out}^c = e_d^p i_d^n + e_q^p i_q^n + e_d^n i_d^p + e_q^n i_q^p = Q_{out}^s \\ P_{out}^s = e_d^p i_q^n - e_q^p i_d^n - e_d^n i_q^p + e_q^n i_d^p = -Q_{out}^c \end{cases} \quad (1\text{-}2)$$

where $\boldsymbol{E}_{dq}^k = e_d^k + je_q^k$ and $\boldsymbol{I}_{dq}^k = i_d^k + ji_q^k$ ($k = p, n$) denote the grid-side voltage and output current vectors of the IIREG. Super-scripts p and n indicate the positive- and negative-sequence components, respectively.

Neglecting the power loss in both the inverter and the inductor-capacitor-inductor (LCL) filter, the active power equation in DC-link is described as:

$$2CU_{dc}\frac{dU_{dc}}{dt} = P_{out} - P_{in} \quad (2)$$

where C and U_{dc} stand for the DC-link capacitance and voltage, respectively. $P_{in} = 2U_{dc}i_{in}$ represents active power supply from the generation unit. During asymmetrical faults, the two-times frequency components P_{out}^c and P_{out}^s included in active power P_{out} yields a DC-link voltage ripple. Such pulsating voltage has detrimental effects on the stability of the inverter's control system and even trip off IIREG from the electrical grid.

In order to ensure that the IIREGs can ride through asymmetrical faults, the oscillating power components P_{out}^c and P_{out}^s should be regulated into zero through the inverter's controllers. Combined with the model (1), the positive and negative current references of the inverter's controllers i_d^{p*}, i_q^{p*}, i_d^{n*}, and i_q^{n*} can be calculated as:

$$\begin{bmatrix} i_d^{p*} \\ i_q^{p*} \\ i_d^{n*} \\ i_q^{n*} \end{bmatrix} = \frac{2}{3D} \begin{bmatrix} e_d^p P_o - e_q^p Q_o \\ e_q^p P_o + e_d^p Q_o \\ -e_d^n P_o - e_q^n Q_o \\ -e_q^n P_o + e_d^n Q_o \end{bmatrix} \quad (3)$$
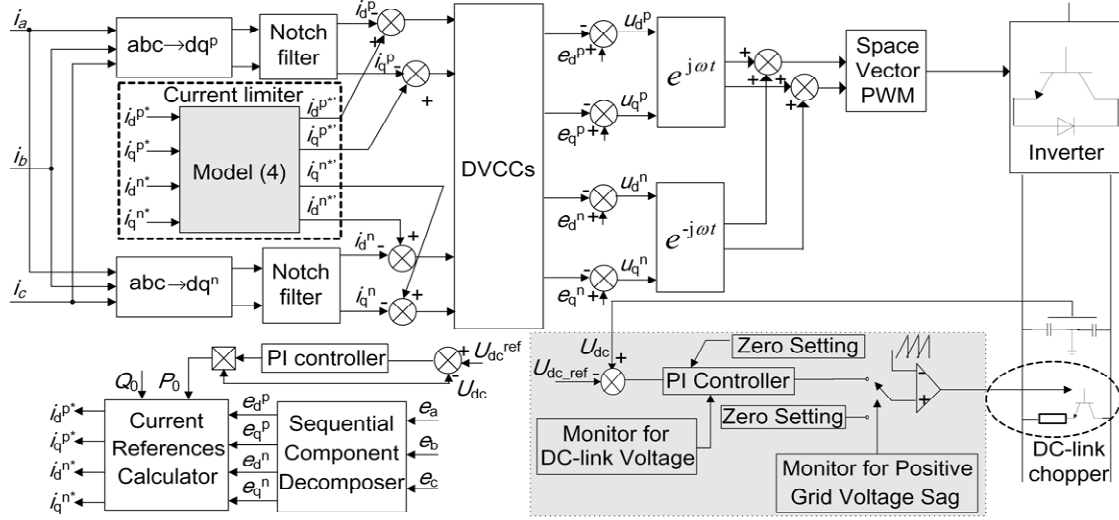
Figure 3. An advanced FRT control strategy.

where Q_o denotes the desired average reactive power that is determined by the FRT requirement of grid code. P_o is the desired average active power. $D = (e_d^p)^2 + (e_q^p)^2 - (e_d^n)^2 - (e_q^n)^2 = |\mathbf{E}_{dq}^p|^2 - |\mathbf{E}_{dn}^p|^2$ becomes larger with the increasing severity of asymmetrical faults. As a result, the current through inverter becomes also higher. The currents may exceed the inverter's maximum allowable current. Hence, the currents through inverter should be regulated within its allowable value. However, if the currents are restrained, the imbalance between the DC-link active input power and the inverter output power may cause a dangerous rise in the DC-link voltage. The following sections will discuss how to co-ordinately solve the inverter over-current and DC-link overvoltage problems.

2.2. Enhanced FRT Strategy

Aimed at the mentioned problems, an advanced FRT control strategy is developed as shown in Figure 3. Different from the traditional strategy based on DVCC (Chong et al., 2008), the studied FRT strategy takes care of both the inverter over-current and DC-link voltage fluctuation. Both a novel current limiter and a DC-link chopper controller are designed, respectively. The corresponding details are explained as follows.

The key idea of the novel current limiter is to fully utilize the inverter's potential capacity to deliver the powers within the inverter's ampere constraint. Firstly, the three-phase current magnitudes I_{am}, I_{bm}, and I_{cm} through inverter are calculated as:

$$\begin{cases} i_a = \left|\mathbf{I}_{dq}^{p*}\right| \sin(\omega t + \theta^p) + \left|\mathbf{I}_{dq}^{n*}\right| \sin(\omega t + \theta^n) \\ i_b = \left|\mathbf{I}_{dq}^{p*}\right| \sin(\omega t - 2\pi/3 + \theta^p) + \left|\mathbf{I}_{dq}^{n*}\right| \sin(\omega t + 2\pi/3 + \theta^n) \\ i_c = \left|\mathbf{I}_{dq}^{p*}\right| \sin(\omega t + 2\pi/3 + \theta^p) + \left|\mathbf{I}_{dq}^{n*}\right| \sin(\omega t - 2\pi/3 + \theta^n) \end{cases} \quad (4\text{-}1)$$

where i_a, i_b, and i_c are instantaneous currents through inverter.

$|\mathbf{I}_{dq}^{k*}| = i_d^{k*} + ji_q^{k*}$ $(k = p, n)$ represents the amplitude of positive- or negative-sequence current vector from current references calculating model (3), respectively. $\theta^p = \arctan(i_q^{p*}/i_d^{q*})$, and $\theta^n = 2\pi - \arctan(i_q^{n*}/i_d^{n*})$ are the phase angles of positive- and negative-sequence current vectors.

Further, the maximum current magnitudes through inverter can be obtained as $I_{max} = \max(I_{am}, I_{bm}, I_{cm})$. If I_{max} is greater than the inverter's ampere constraint I_{lim}, the positive- and negative-sequence current references are recalculated as:

$$i_j^{k*\prime} = i_j^{k*} I_{lim}/I_{max} = \alpha i_j^{k*} \quad (4\text{-}2)$$

where subscript j denotes the d- or q-axis component. $\alpha = I_{lim}/I_{max}$ is the scalar coefficient of current limiter. $\alpha < 1$ if $I_{max} > I_{lim}$.

By substituting Model (4-2) into (1-2), we find that the DC-link voltage fluctuation can still be eliminated although the current references are reset. In addition, three-phase currents provided by IIREG are sinusoidal even if the current limiter is applied. However, due to the current limiter activation, active power through the inverter is limited. It leads to the DC-link over-voltage.

In order to solve the DC-link overvoltage problem, the DC-link chopper is engaged. The controller is designed for the DC-link chopper as shown in the bottom right of Figure 3. The PI controller is automatically enabled once the positive-sequence component of grid-side voltage drops below a critical threshold (0.9 per unit (p.u.)). To timely prevent DC-link over-voltage risks, the integral part of PI controller is activated and reset to the difference between most recent measurement of the DC-link voltage and its reference U_{dc}^{ref} when the actual DC-link voltage is greater than 1.05 p.u. At the same time, the reference of PI controller is equal to that of the inverter's voltage control loop. It can realize a smooth switching between the inverter's control and the chopper's control once a grid fault

occurs.

For the advanced control strategy, a novel current limiter is proposed to avoid the inverter over-current problem under severe faults. At the same time, the chopper PI controller is designed for solving DC-link over-voltage problems. With the proposed FRT strategy, the operation region of IIREGs can effectively enlarged under grid faults. The FRT tests will be further discussed in Section 5.2.

3. Relationship between the Inverter's Control and the IIREGs' Fault Current

To reveal the IIREGs' fault current characteristics, the interaction between the grid-tied inverter's FRT control and the IIREGs' fault current is discussed in the section. When an asymmetrical grid fault occurs, the grid-side voltage of the IIREG is inevitably altered. The negative-sequence component of grid-side voltage is abruptly produced, and the positive-sequence voltage is decreased. As a result, output current of the IIREG is also changed quickly. However, the positive- and negative-sequence component references of current controller (as shown in Figure 3) remain unchanged during the initial periods of the faults (approximately $1 \sim 2$ cycles). Taking the positive-sequence d-axis current control loop for example, its control diagram represented in the form of fault component is shown in Figure 4.
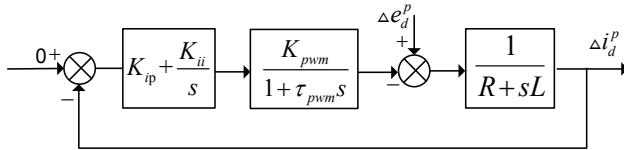

Figure 4. Control Block of d-axis current component.

The corresponding closed-loop transfer function can be expressed as:

$$\frac{\Delta i_d^p(s)}{\Delta e_d^p(s)} = \frac{s(1+\tau_{pwm}s)}{s(R+Ls)(\tau_{pwm}s+1) - k_{pwm}(k_{ip}s+k_{ii})} \quad (5)$$

in which Δi_d^p is the fault component of positive-sequence d-axis current through the inverter. Δe_d^p is the fault component of pos-itive-sequence d-axis grid-side voltage. k_{ip} and k_{ii} are the pro-portional and integral gains of current controller. k_{PWM} is the inverter's equivalent gain. τ_{PWM} is the equivalent time constant of the inverter and its modulation controller. $R = R_1 + R_2$, and $L = L_1 + L_2$. R_1 and L_1 are the equivalent resistance and inductance of the inverter-side reactor of the LCL filter, respectively. R_2 and L_2 denote the resistance and inductance of the grid-side re-actor of the filter.

Model (5) has three poles. Considering the tradeoff be-

tween the system stability and its dynamic tracking performance, the model (5) should include a pair of conjugate poles $(-\zeta\omega_n \pm j\omega_n\sqrt{1-\xi^2}$, the damping ratio ξ is generally about 0.707, ω_n is the natural frequency). The conjugate poles have the smallest real component among all poles, and they can play a leading role in dynamic behavior of the current control loop. Assuming that the abrupt change of the voltage e_d^p is Δe_d^p caused by an asymmetrical fault, in the time domain the corresponding transient current component of the conjugate poles can be expressed as:

$$\Delta i_d^p(t) = -1.4\Delta e_d^p e^{-0.7\omega_n t} \sin(0.7141\omega_n t + 0.7855) \quad (6\text{-}1)$$

in which the natural frequency ω_n satisfies the following equation.

$$\begin{cases} 1.4L\omega_n a^2 - k_{pwm}k_{ip}a + k_{pwm}\tau_{pwm}k_{ii} = 0 \\ a = 1 - 1.4\tau_{pwm}\omega_n \end{cases} \quad (6\text{-}2)$$

According to the model (6-1), the positive-sequence d-axis transient current decays periodically. The transient current is related not only with the grid-side voltage variation Δe_d^p, but also closely with the PI controller's gains, the inverter's equivalent parameters, the LCL filter's equivalent parameters and so on. In fact, the positive-sequence q-axis transient current as well as the negative-sequence d- and q-axis transient currents have similar rules. Thus, during the first $1 \sim 2$ cycles of a fault, the output current of IIREGs is closely associated with on the inverter controllers' parameters.

After the initial periods of the faults (approximately $1 \sim 2$ cycles), the reference values of the current controller are altered by the inverter's average power references. It also causes that the output current from IIREGs has short transients. The transient components depend on the parameters of the current controllers, the inverter's and grid-tie filter's main circuit.

If the asymmetrical faults are severe, the output current of IIREGs may reach the inverter's maximum allowable value. As a result, the current limiter and DC-link chopper circuit are activated. In this scenario, the transient process for IIREGs becomes more complicated. The transient current characteristics of the IIREGs are affected alternatively by different control loops of the IIREGs, involving the inverter's controllers and the current limiter as well as the DC-link chopper's controller. These controllers are generally nonlinear. It becomes difficult to describe the transient current characteristics by using definite mathematical models.

Whereas, the length of the IIREGs' transient process is less than $3 \sim 4$ cycles due to the fast response of the grid-tie inverter's control or DC-link chopper's control. After the transient process, the IIREGs go into a steady-state operation mode. In the steady-state periods, the fault currents from the IIREGs are closely related with the FRT goals, independent of the employed inverter's controller and its parameters. Thus, it becomes possible to derive the expression of IIREG's fault current without the inverter control strategies.

4. Steady-State Short-Circuit Current Model for IIREGs

According to the FRT control goal, the positive- and negative-sequence amplitudes of steady-state fault current from the IIREGs can be expressed as follows (in a p.u. system):

$$\begin{cases} I_m^p = |\boldsymbol{I}_{dq}^p| = |\boldsymbol{E}_{dq}^p| S_o \Big/ \Big(|\boldsymbol{E}_{dq}^p|^2 - |\boldsymbol{E}_{dq}^n|^2 \Big) = S_o \Big/ \Big(\gamma E_{mN} \big(1 - \beta^2\big) \Big) \\ I_m^n = |\boldsymbol{I}_{dq}^n| = |\boldsymbol{E}_{dq}^n| S_o \Big/ \Big(|\boldsymbol{E}_{dq}^p|^2 - |\boldsymbol{E}_{dq}^n|^2 \Big) = \beta S_o \Big/ \Big(\gamma E_{mN} \big(1 - \beta^2\big) \Big) \end{cases} \quad (7\text{-}1)$$

where $|\boldsymbol{E}_{dq}^p|$ and $|\boldsymbol{E}_{dq}^n|$ are the positive- and negative-sequence amplitudes of grid-side voltage. γ reflects the drop coefficient of positive-sequence grid-side voltage. $\beta = |\boldsymbol{E}_{dq}^n|/|\boldsymbol{E}_{dq}^p|$ denotes the imbalance degree of grid-side voltage. E_{mN} is the rated grid-side voltage magnitude. S_o represents the apparent power injected into the grid during the faults, it can be expressed as:

$$S_o = \begin{cases} \sqrt{P_o^2 + Q_o^2} & \alpha \geq 1 \\ \alpha \sqrt{P_o^2 + Q_o^2} & \alpha < 1 \end{cases} \quad (7\text{-}2)$$

From the model (7-1), the IIREGs can generate the negative-sequence currents. The fault current characteristic is different from that of the synchronous generators.

In addition, according to the model (4-1), the three-phase short-circuit current amplitudes I_{am}, I_{bm}, and I_{cm} from IIREGs can be calculated as:

$$\begin{cases} I_{am} = \Big(S_o \Big/ \gamma E_m^p \big(1 - \beta^2\big) \Big) \sqrt{1 + \beta^2 + 2\beta \cos \theta_i} \\ I_{bm} = \Big(S_o \Big/ \gamma E_m^p \big(1 - \beta^2\big) \Big) \sqrt{1 + \beta^2 + 2\beta \cos \big(\theta_i - 4\pi/3 \big)} \\ I_{cm} = \Big(S_o \Big/ \gamma E_m^p \big(1 - \beta^2\big) \Big) \sqrt{1 + \beta^2 + 2\beta \cos \big(\theta_i + 4\pi/3 \big)} \end{cases} \quad (8)$$

in which $\theta_i = \tan^{-1}(e_q^n/e_d^n) - 2\pi$. The angle θ_i is closely related with negative-sequence grid-side voltage. Given the positive and negative current amplitude I_m^k $(k = p, n)$, the three phase current peaks vary periodically with θ_i. If θ_i is equal to 0, $3\pi/4$, or $5\pi/4$, the current magnitude in phases a, b, or c is respecttively the largest. The maximum peak is equal to the magnitude sum of the positive- and negative-sequence current vectors.

From the model (8), it is found that the short-circuit current provided by IIREGs is determined by two factors. The one is closely related with the apparent power delivered to grid. The power is determined by FRT control goal that is a fixed value for the specified grid code. The other is the positive- and negative-sequence grid-side voltage vectors. The vectors depend on both the equivalent short-circuit parameters of a connected grid and the grid fault conditions. The equivalent parameters and the fault conditions should be given from the perspective of the study on the relay protection. Thus, the steady-state short-circuit current model of IIREGs as shown in model (8) is

independent of the inverter's controllers and its parameters. The fault current values can be obtained without knowing the inverter's control strategies. It can provide possibility of calculating the relay protection settings for the electrical grid with larger-scale IIREGs.

5. FRT Capability Tests and Short-Circuit Current Model Verification

5.1. Experimental Test Rig

This section presents the experimental test rig, which serves as the basis for testing the proposed FRT strategy and verifying the short-circuit current model of IIREGs.
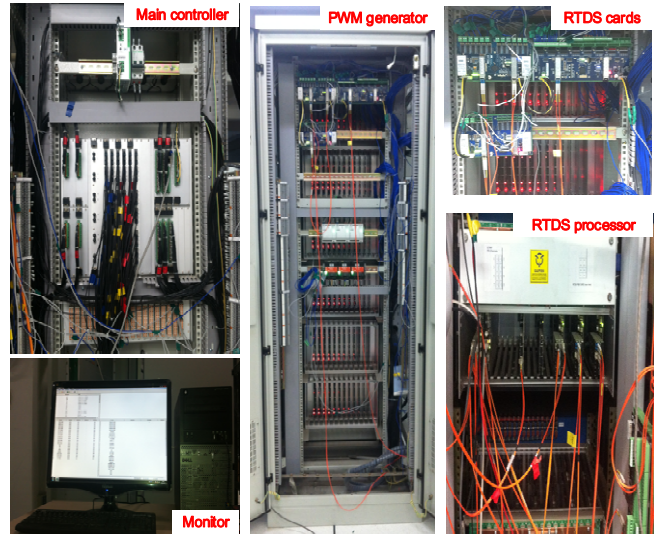

Figure 5. Physical layout of the experimental test bench.

As shown in Figure 5, the experimental test rig consists of main controller, pulse-width-modulated (PWM) generator, real time digital simulator (RTDS) and monitor. These hardware's performance indicators are devised according to the corresponding international standards or the marketable product's design criteria. In the test rig, the main controller is basically composed of the Digital Signal Processor (DSP) / Field Programmable Gate Array (FPGA) combined control boards. It can implement the control and protection algorithms of the IIREG system based on the modular programming method. The algorithm codes can be flexibly modified. PWM generator is used for generating the electrical firing signals for the inverters. RTDS simulator is employed to simulate the main circuit of electrical grid with the tested IIREG. Monitor can be utilized for starting and stopping the IIREG system, so as to reset the control and protection parameters and so on.

Based on the experimental rig, the detailed test model is built as shown in Figure 6. The topology is typical, and it has been widely used for the transmission grid with the large-scale IIREGs. The related parameters are listed in the Appendix, which are mostly based on the information from industries and literatures.
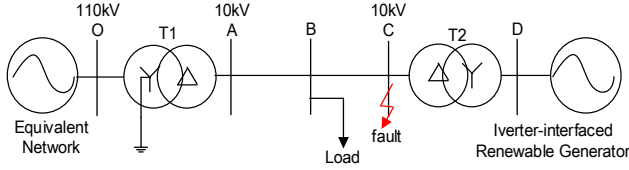
Figure 6. Test bed system with an inverter-interfaced renewable energy generator.

5.2. FRT Capability Tests

In order to test FRT capability of the IIREGs, it is assumed that a two-line-to-ground fault (TLGF) occurs between phases a and b in bus C at t = 0.6 s and lasts for 0.65 s. The pre-fault IIREG operates at its rated state. After the fault, the positive-sequence grid-side voltage falls from 1.02 to 0.57 p.u., and the negative-sequence voltage shoots up to 0.55 p.u. Figure 7 shows the test results of an IIREG with the proposed FRT control strategy and conventional DVCC strategy.

From Figures 7 (c) and (d), the IIREG with conventional DVCC strategy becomes unstable after the fault. The maximum DC-link voltage reaches approximately 3.75 p.u. And the maximum value of three-phase currents through inverter is about 7.5 p.u. It results in the over-voltage and over-current protection trip. The IIREG will be cut off from the electrical grid. It does not conform with the FRT requirement of grid code.

However, as shown in Figures 7 (a) and (b), the proposed FRT strategy can ensure stable operation of the IIREG during the aforementioned fault. Both three-phase currents through inverter and DC-link voltage are kept within their acceptable limits. The results indicate that the proposed control strategy can effectively enlarge the region of riding through grid faults. It was established that the proposed FRT strategy can help the IIREGs to ride through the asymmetrical faults that causes a 96% imbalanced grid-side voltage ($|\boldsymbol{E}_{dq}^{n}|/|\boldsymbol{E}_{dq}^{p}|$). In fact, the proposed strategy can be also applied for the severe symmetrical faults. Owing to space constraints, the corresponding tests are not discussed here.

5.3. Verification for Steady-State Short-Circuit Current Model

To verify the IIREG's short-circuit current model, both the calculation results based on Matlab and the test results based on the experimental rig are compared and analyzed. In addition, the calculation results are from the existing model (Jia et al., 2017) and the models used in this paper. Table 1 shows the comparison results with different active and reactive power commands. Here, it is assumed that a bolted TLGF occurs in bus C. The fault is the same with the one discussed in Section 5.3. Before the fault the IIREG operates at its rated state, and its output current is approximately 1.245 kA.
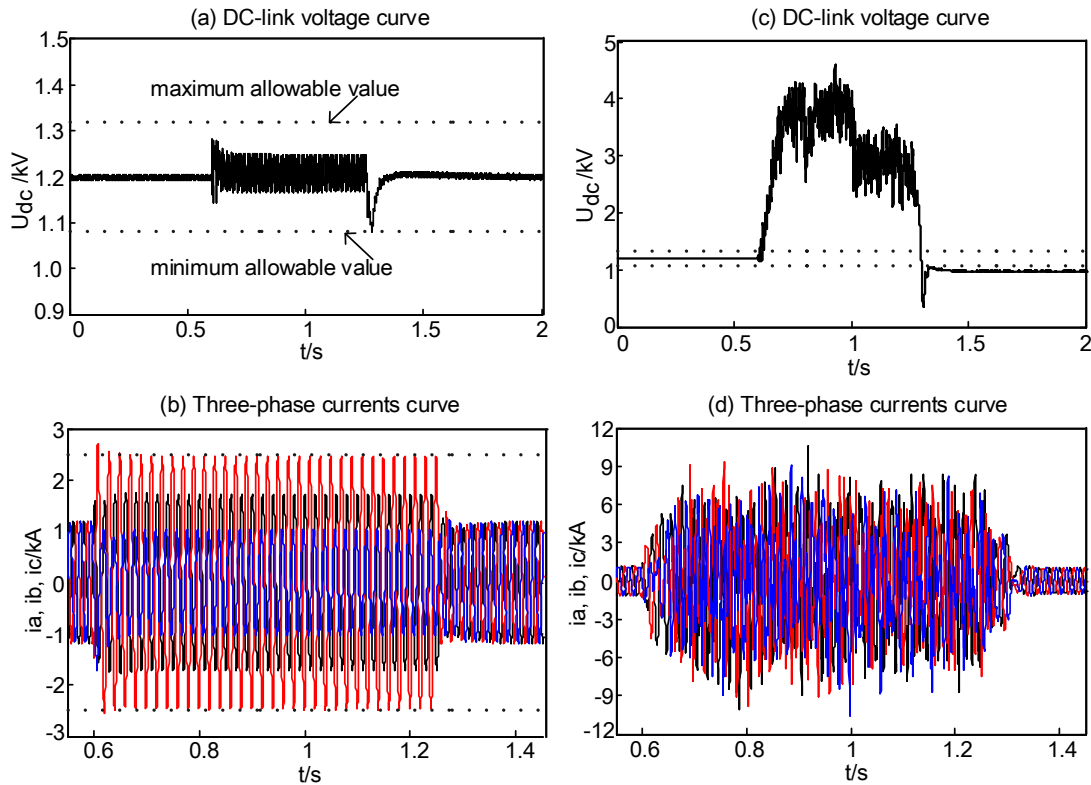

Figure 7. Test results with different strategies: (a) DC-link voltage with the proposed FRT strategy; (b) DC-link voltage with the conventional DVCC strategy; (c) Three-phase currents with the proposed FRT strategy; (d) Three-phase currents with the conventional DVCC strategy.

Table 1. Fault Currents Results of IIREGs with Different Active and Reactive Power Commands

		P_o = 1 p.u. Q_o = 1 p.u.			P_o = 1 p.u. Q_o = 0.1 p.u.			P_o = 0 p.u. Q_o = 1 p.u.		
Current amplitude		I_{am}	I_{bm}	I_{cm}	I_{am}	I_{bm}	I_{cm}	I_{am}	I_{bm}	I_{cm}
Test results		1.81 kA	2.49 kA	1.25 kA	2.43 kA	2.49 kA	0.31 kA	1.50 kA	2.49 kA	1.55 kA
Proposed model	Calculation results	1.76 kA	2.45 kA	1.19 kA	2.46 kA	2.46 kA	0.33 kA	1.48 kA	2.44 kA	1.60 kA
	Relative error	-2.76 %	-1.60 %	-4.80 %	1.23 %	-1.22 %	6.45 %	-1.33 %	-2.05 %	3.22 %
Existing model	Calculation results	2.69 kA	3.7 kA	1.86 kA	2.59 kA	2.59 kA	0.35 kA	1.52 kA	2.51 kA	1.65 kA
	Relative error	48.62 %	48.6 %	48.8 %	6.58 %	4.02 %	12.9 %	1.33 %	0.8 %	6.45 %

From Table 1, it is found that the difference between the calculation results and test results is very small based on the proposed model. The maximal error value reaches 6.45%, only when the desired powers of grid-tie inverter are P_o = 1 p.u., Q_o = 0.1 p.u. Under the other power commands, the errors are less than 5%. It is indicated that the proposed IIREG's fault current model as shown in the model (8) has high accuracy. By comparison, in Table 1 there are great relative errors between calculation results of the existing model and test results. The maximal error value reaches 48.8%. It is because that the existing calculation model ignores the effect of grid-tied inverter current constraint. From Table 1, with different desired powers, the phase current amplitudes from the existing model always exceed the inverter's maximum allowable current (2.49 kA). Only when the desired powers of grid-tie inverter are P_o = 0 p.u., Q_o = 1 p.u., the relative error is smaller due to the minimum difference between the current amplitudes from the existing model and the inverter's maximum allowable current.

Moreover, compared with the tested three-phase fault currents results, it is found that the relationship between the current amplitudes is different under various active and reactive power commands. Although in all condition the faulty phase b current magnitude reaches the inverter's ampere constraint (2 p.u., 2.49 kA), the relationship between the phase a and c current amplitudes is affected by the actual real and reactive power commands. Therefore, the active and reactive power commands for grid-tie inverter affect not only the amplitude values of IIREG's fault currents but also the relationship of the three-phase current amplitudes. The fault current characteristic of IIREG is different from that of synchronous generators. The fault current of synchronous generators is mainly influenced by the machine equivalent impedance. Whereas, the impedance is not associated with the generators' active and reactive injections.

6. Conclusions

In order to reveal the IIREGs' fault current characteristics and propose their fault current calculation model, an advanced FRT control strategy is firstly proposed in this paper. The control strategy can coordinately solve the inverter overcurrent and DC-link overvoltage problem. It has been demonstrated that the IIREGs with the proposed strategy can ride-through the severe asymmetrical faults (the imbalance of grid-side voltage is about 100%). On the basis of this, the interaction between the inverter's control strategies and the IIREGs' short-circuit current characteristics are analyzed. It is revealed that the inverter's control structures and the corresponding parameters only affect the transient fault current and not the steady-state short-circuit current. And the steady-state fault currents are closely related with FRT goals and the inverter' ampere constraint. Further, the steady-state fault current calculation model of IIREGs is derived, which is independent of the inverter's control strategies. The model makes it possible to calculate the steady-state fault current from IIREGs without the inverter control strategies. The results are useful for assessing and improving the protection schemes of the electrical grid with lots of IIREGs.

Appendix

Transformer T_1 ratio n = 10.5/2.2 kV; transformer T_2 ratio n = 121/10.5 kV; the line length AB = 5.5 km and BC = 1.6 km; grid frequency ω = 50 Hz; Grid-tie inverter: rated capacity S = 1.5 MW, rated current = 1.245 kA; DC-link capacitor C = 4500 μF, DC-link voltage U_{dc} = 1.2 kV; LCL filter: L_1 = 1100 μH, L_2 = 123.55 μH, C_f = 200 μF, R_f = 0.2484 Ω; inner positive or negative current controller: proportional gain K_{iP} = 0.3285 p.u., integral time constant T_{iI} = 0.0175 p.u.; outer voltage controller: K_{vP} = 0.75 p.u., T_{vI} = 0.875 p.u.

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